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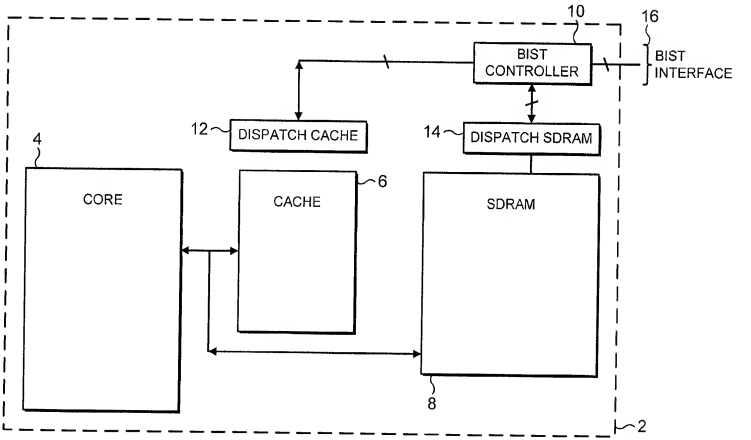

FIG. 1

Inventor: SLOBODNIK et al
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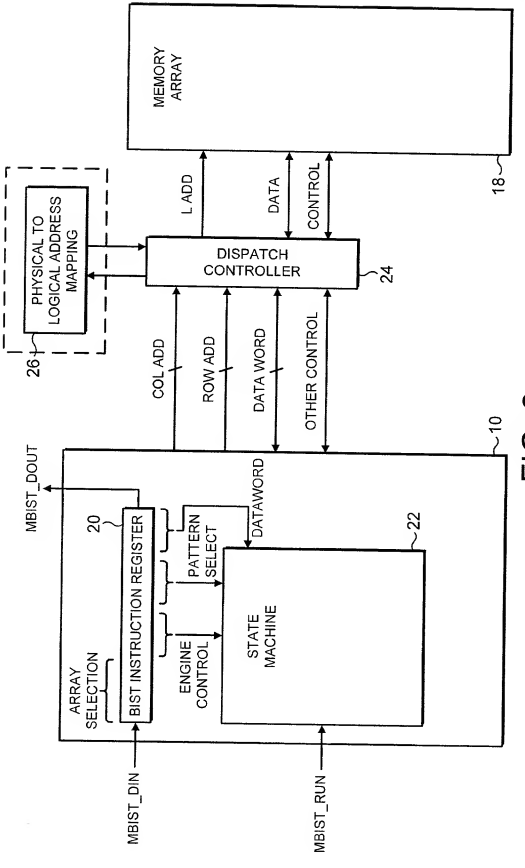

FIG. 2

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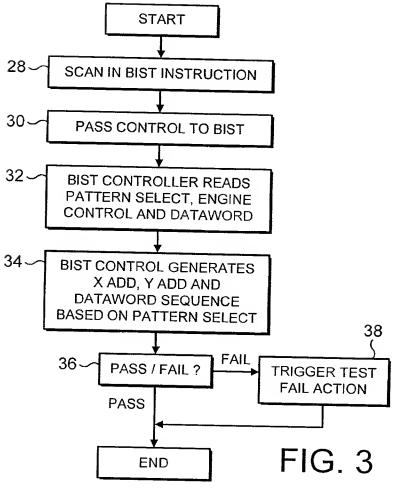
START
28
SCAN IN BIST INSTRUCTION
30
PASS CONTROL TO BIST
32
BIST CONTROLLER READS PATTERN SELECT, ENGINE CONTROL AND DATAWORD
34
BIST CONTROL GENERATES X ADD, Y ADD AND DATAWORD SEQUENCE BASED ON PATTERN SELECT
38
36
PASS / FAIL ?
FAIL
TRIGGER TEST FAIL ACTION
PASS
END

FIG. 3

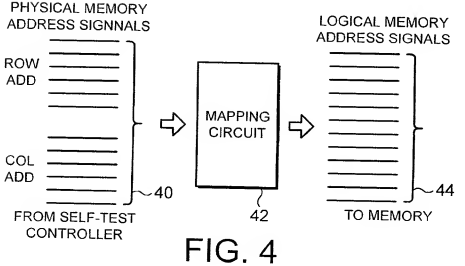
PHYSICAL MEMORY ADDRESS SIGNNALS
ROW ADD
COL ADD
40
FROM SELF-TEST CONTROLLER
MAPPING CIRCUIT
42
LOGICAL MEMORY ADDRESS SIGNALS
44
TO MEMORY

FIG. 4

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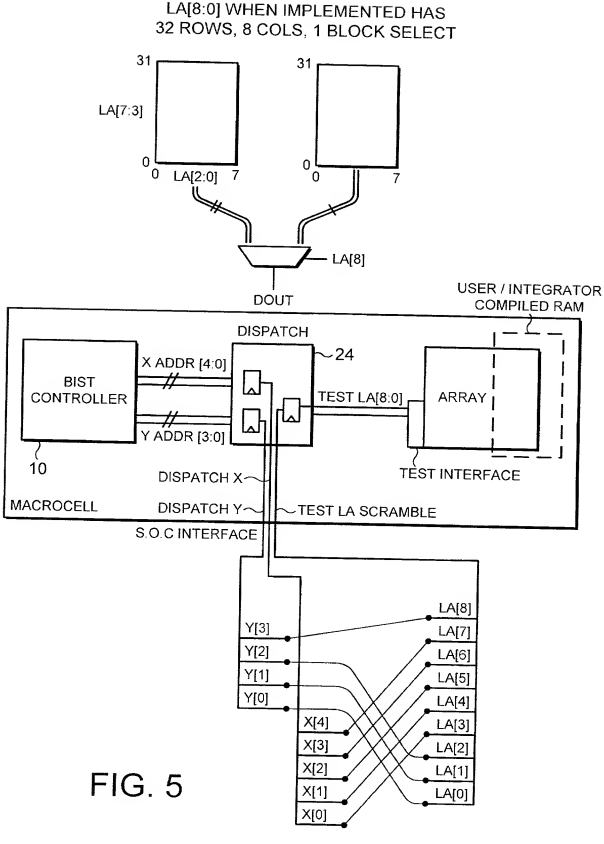

FIG. 5